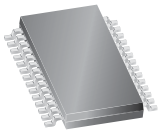
Automotive DMOS Microstepping Driver with Translator

Features and Benefits

- Typical application up to ±1 A, 35 V output rating
- Low $R_{DS(ON)}$ outputs, 0.67 Ω source, 0.54 Ω sink typical
- Automatic current decay mode detection/selection
- 3.0 V to 5.5 V logic supply voltage range
- Mixed, fast, and slow current decay modes
- Synchronous rectification for low power dissipation
- Internal OVLO, UVLO, and thermal shutdown circuitry
- Crossover current protection
- Short to supply/ground and short/low load current diagnostics

Package: 28 pin TSSOP with exposed thermal pad (suffix LP)



Approximate Size

Description

The A3980 is a complete microstepping motor driver with built-in translator for easy operation. It is designed to operate bipolar stepper motors in full-, half-, eighth-, and sixteenth-step modes, at up to 35 V and ±1 A. The A3980 includes a fixed off-time current regulator which has the ability to operate in slow, fast, or mixed decay modes. This results in reduced audible motor noise, increased step accuracy, and reduced power dissipation.

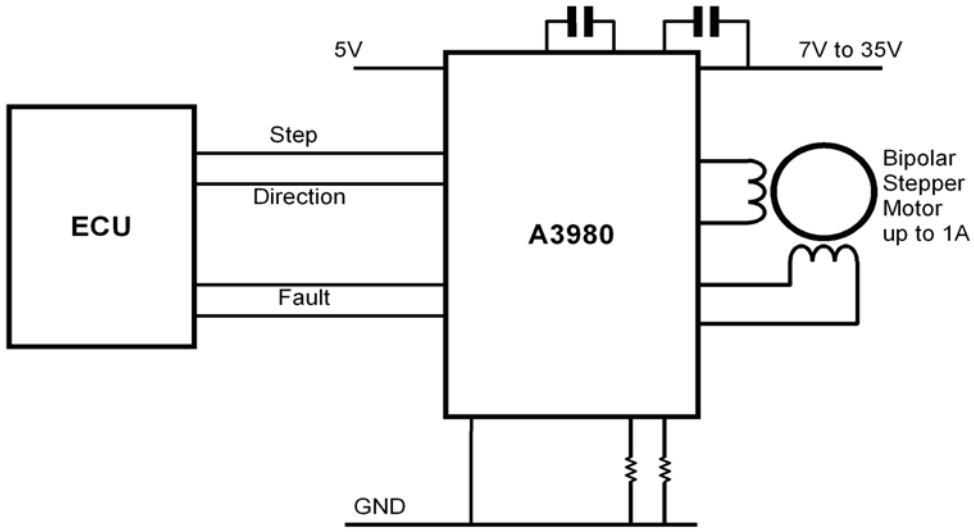
The translator is the key to the easy implementation of the A3980. Simply inputting one pulse on the step input drives the motor one microstep. There are no phase sequence tables, high frequency control lines, or complex interfaces to program. The A3980 interface is an ideal fit for applications where a complex µP is unavailable or overburdened.

Internal synchronous rectification control circuitry is provided to improve power dissipation during PWM operation.

Internal circuit protection includes: thermal shutdown with hysteresis, overvoltage lockout (OVLO), undervoltage lockout (UVLO), and crossover current protection. Special power-up sequencing is not required. In addition, two diagnostic fault flags provide indication of shorts or opens on the motor windings.

The A3980 is supplied in a low-profile (1.1 mm) 28L TSSOP with exposed thermal pad. This device is available also in a lead-free version (leadframe plating 100% matte tin).

Typical Application



Selection Guide

Part Number	Pb-free	Packing
A3980KLP	–	50 pieces per tube
A3980KLP-T	Yes	
A3980KLPTR	–	4000 pieces per reel
A3980KLPTR-T	Yes	

Absolute Maximum Ratings

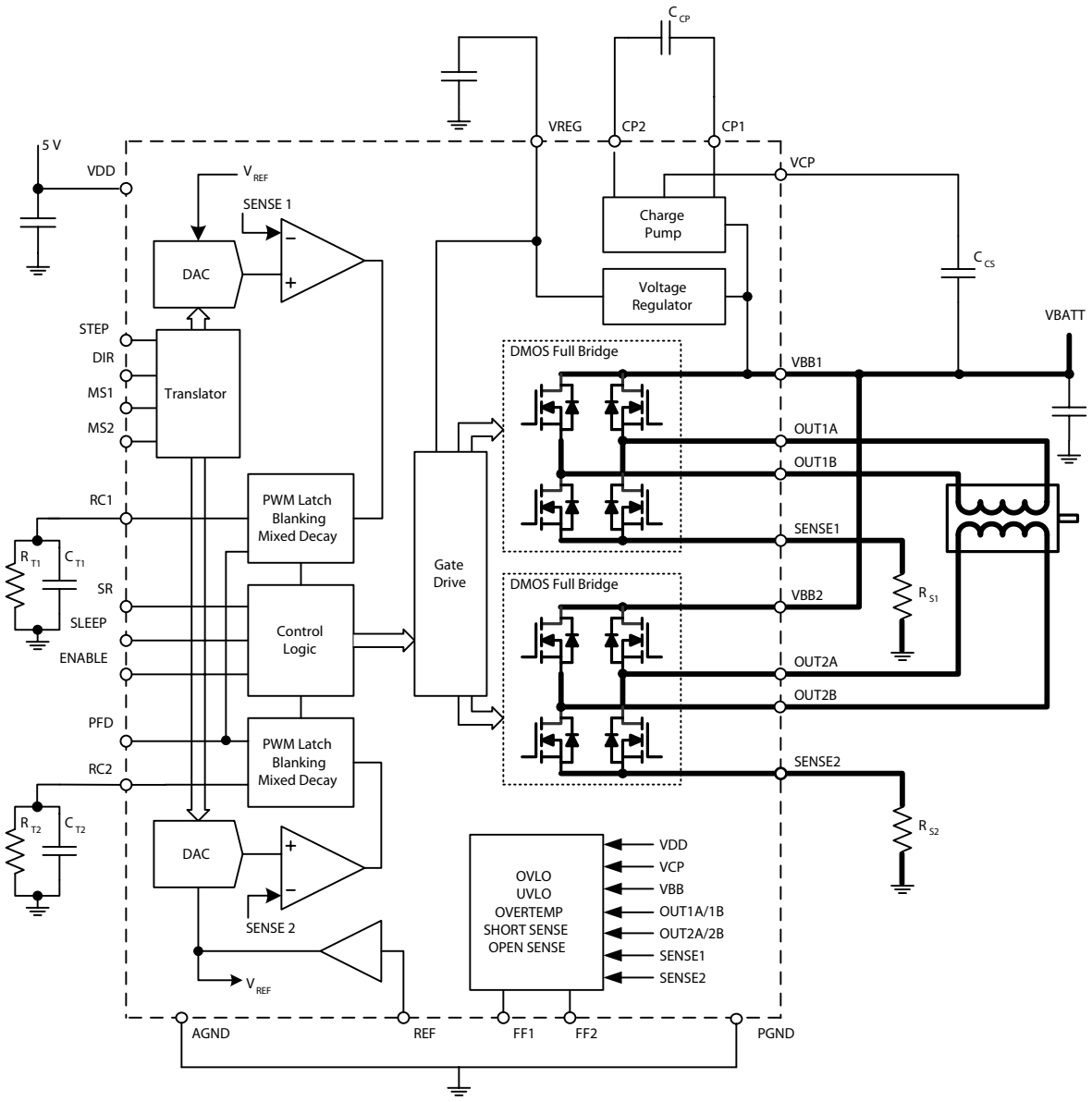
Characteristic	Symbol	Notes	Rating	Units
Load Supply Voltage	V_{BB}	500 ms	50	V
Logic Supply Voltage	V_{DD}		7.0	V
Logic Input Voltage	V_{IN}		–0.3 to V_{DD} + 0.3	V
		(t_W < 30 ns)	–1.0 to V_{DD} + 1	V
Sense Voltage	V_{SENSE}		0.5	V
Reference Voltage	V_{REF}		0 to V_{DD}	V
Operating Ambient Temperature	T_A	Range K	–40 to 125	°C
Maximum Junction Temperature	T_J(max)		150	°C
Storage Temperature	T_{stg}		–55 to 150	°C
ESD Rating - Human Body Model		AEC-Q100-002, all pins	2.0	kV
ESD Rating - Charged Device Model		AEC-Q100-011, all pins	1.0	kV

Thermal Ratings

Characteristic	Symbol	Test Conditions*	Value	Units
Package Thermal Resistance	$R_{\theta JA}$	2-layer PCB with 3.8 in.^{2} of copper area each side connected by thermal vias	32	ºC/W
		4-layer PCB based on JEDEC standards	28	ºC/W

*Additional thermal information available on Allegro Web site.

Functional Block Diagram



ELECTRICAL CHARACTERISTICS at T_J = –40°C to +150ºC, V_{BB} = 14 V, V_{DD} = 3.0 to 5.5 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
Output Drivers						
Load Supply Voltage Range	V_{BB}	Driving Operating Sleep mode	8 7 0	— — —	V_{OVB} 50 35	V V V
Output Leakage Current[2]	I_{DSS}	V_{OUT} = V_{BB} V_{OUT} = 0 V	—	< 1.0 < 1.0	20 –20	µA µA
Output-On Resistance	R_{DSON}	Source driver, I_{OUT} = –1 A, T_A < 25ºC Sink driver, I_{OUT} = 1 A, T_A < 25ºC	—	0.51 0.45	0.86 0.65	Ω Ω
		Source driver, I_{OUT} = –1 A, T_A < 125ºC Sink driver, I_{OUT} = 1 A, T_A < 125ºC	—	0.87 0.72	1.06 0.83	Ω Ω
Body Diode Forward Voltage	V_F	Source diode, I_F = –1 A Sink diode, I_F = 1 A	—	—	1.4 1.4	V V
Motor Supply Current	I_{BB}	f_{PWM} < 50 kHz Operating, outputs disabled Sleep mode	—	—	8 6 20	mA mA µA
Logic Supply Current	I_{DD}	f_{PWM} < 50 kHz Outputs off Sleep mode	—	—	12 10 20	mA mA µA
Logic Interface						
Logic Supply Voltage Range	V_{DD}	Operating	3.0	5.0	5.5	V
Input Low Voltage	V_{IL}	—	—	—	0.3 V_{DD}	V
Input High Voltage	V_{IH}	—	0.7 V_{DD}	—	—	V
Input Hysteresis	V_{IHYS}	—	200	300	500	mV
Input Current[2]	I_{IN}	—	–20	< ±1	20	µA
Output Low Voltage	V_{OL}	I_O = 3 mA	—	—	0.4	V
Output High Voltage	V_{OH}	I_O = –200 µA	2.8	—	—	V
STEP Pin Low	t_{STPL}	—	1	—	—	µs
STEP Pin High	t_{STPH}	—	1	—	—	µs
Setup Time for Input Change to STEP	t_{SU}	MS1, MS2, DIR	200	—	—	ns
Hold Time for Input Change from STEP	t_H	MS1, MS2, DIR	200	—	—	ns
Wake-Up Time from SLEEP	t_{EN}	—	—	—	1	ms

Continued on next page

ELECTRICAL CHARACTERISTICS (*continued*) at T_J = –40°C to +150ºC, V_{BB} = 14 V, V_{DD} = 3.0 to 5.5 V (unless otherwise noted)

Characteristics	Symbol	Test Conditions	Min.	Typ.[1]	Max.	Units
Current Control						
Blank Time	t_{BLANK}	R_T = 56 K , C_T = 680 pF	700	950	1200	ns
Fixed Off Time	t_{OFF}	R_T = 56 K , C_T = 680 pF	30	38	46	µs
Mixed Decay Trip Points	PFD_H PFD_L	—	—	0.60 V_{DD} 0.21 V_{DD}	—	V
Crossover Dead Time	t_{DT}	—	100	475	800	ns
Recommended Reference Input Voltage	V_{REF}	—	0.8	—	4	V
Reference Input Current[2]	I_{REF}	—	–3	0	3	µA
Current Trip-Level Error[3]	err_I	2 V < V_{REF} < 4 V, $\%I_{TripMAX}$ = 38% 2 V < V_{REF} < 4 V, $\%I_{TripMAX}$ = 70% 2 V < V_{REF} < 4 V, $\%I_{TripMAX}$ = 100%	—	—	±15 ±10 ±5	%
Thermal Protection						
Thermal Shutdown	T_{SD}	—	160	170	180	ºC
Thermal Shutdown Hysteresis	T_{SDH}	—	—	15	—	ºC
Diagnostics						
Max V_{DS} on High-Side Bridge FETs	V_{DSHT}	Sampled after t_{BLANK} + t_{SCT}	—	1.5	—	V
Max V_{DS} on Low-Side Bridge FETs	V_{DSLT}	Sampled after t_{BLANK} + t_{SCT}	—	1.5	—	V
V_{DS} Fault Measurement Delay	t_{SCT}	—	—	700	—	ns
Minimum Load Current	I_{OC}	w.r.t. $I_{TRIPMAX}$ at Home position	—	35	—	%
V_{BB} Overvoltage Lockout	V_{OVB}	V_{BB} rising	32	34	36	V
V_{BB} Overvoltage Lockout Hysteresis	V_{OVBH}	—	2	—	4	V
V_{REG} Undervoltage Lockout	V_{UVR}	V_{REG} falling	5.3	5.7	6.0	V
V_{DD} Enable Threshold	V_{UVD}	V_{DD} rising	2.45	2.7	2.95	V
V_{DD} Enable Threshold Hysteresis	V_{UVDH}	—	50	100	—	mV

[1]Typical data are for initial design estimations only, and assume optimum manufacturing and application conditions. Performance may vary for individual units, within the specified maximum and minimum limits.

[2]Negative current is defined as coming out of (sourcing from) the specified device pin.

[3]$err_I = (I_{Trip} – I_{Prog}) / I_{Prog}$, where $I_{Prog} = \%I_{TripMAX} \times I_{TripMAX}$.

Logic Interface Timing Diagram

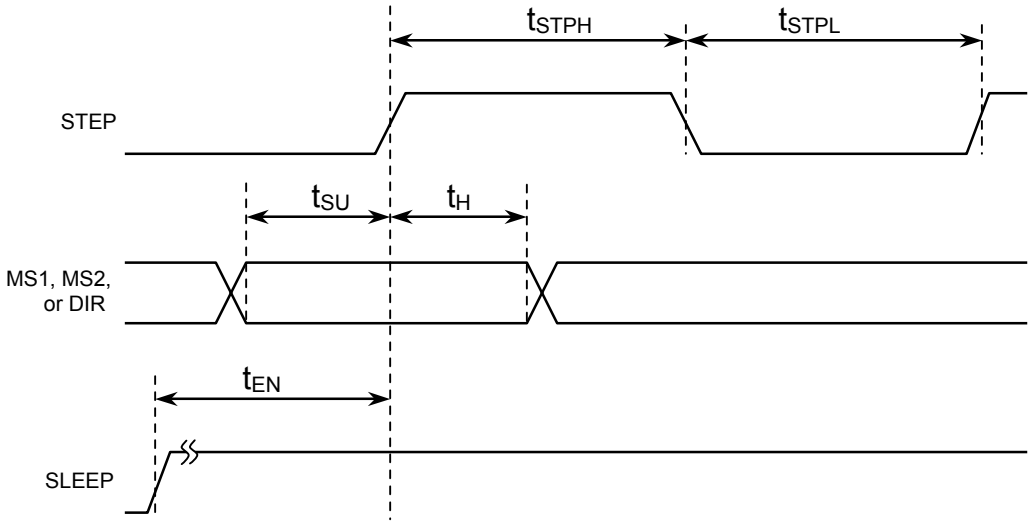


Table 1. Microstep Resolution Truth Table

MS1	MS2	Microstep Resolution
L	L	Full Step
H	L	Half Step
L	H	Eighth Step
H	H	Sixteenth Step

Table 2. Fault Report by Fault Flags

FF1	FF2	Fault
L	L	UVLO, OVLO, Overtemperature, Low Load Current, or Shorted Load
H	L	Short to Ground
L	H	Short to Supply
H	H	None

Table 3. Step Sequencing Settings

Home microstep position at Step Angle 45°; DIR = H

Full Step #	Half Step #	1/8 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (°)	Full Step #	Half Step #	1/8 Step #	1/16 Step #	Phase 1 Current [% $I_{tripMax}$] (%)	Phase 2 Current [% $I_{tripMax}$] (%)	Step Angle (°)
	1	1	1	100.00	0.00	0.0		5	17	33	–100.00	0.00	180.0
			2	99.52	9.80	5.6				34	–99.52	–9.80	185.6
		2	3	98.08	19.51	11.3			18	35	–98.08	–19.51	191.3
			4	95.69	29.03	16.9				36	–95.69	–29.03	196.9
		3	5	92.39	38.27	22.5			19	37	–92.39	–38.27	202.5
			6	88.19	47.14	28.1				38	–88.19	–47.14	208.1
		4	7	83.15	55.56	33.8			20	39	–83.15	–55.56	213.8
			8	77.30	63.44	39.4				40	–77.30	–63.44	219.4
1	2	5	9	70.71	70.71	45.0	3	6	21	41	–70.71	–70.71	225.0
			10	63.44	77.30	50.6				42	–63.44	–77.30	230.6
		6	11	55.56	83.15	56.3			22	43	–55.56	–83.15	236.3
			12	47.14	88.19	61.9				44	–47.14	–88.19	241.9
		7	13	38.27	92.39	67.5			23	45	–38.27	–92.39	247.5
			14	29.03	95.69	73.1				46	–29.03	–95.69	253.1
		8	15	19.51	98.08	78.8			24	47	–19.51	–98.08	258.8
			16	9.80	99.52	84.4				48	–9.80	–99.52	264.4
	3	9	17	0.00	100.00	90.0		7	25	49	0.00	–100.00	270.0
			18	–9.80	99.52	95.6				50	9.80	–99.52	275.6
		10	19	–19.51	98.08	101.3			26	51	19.51	–98.08	281.3
			20	–29.03	95.69	106.9				52	29.03	–95.69	286.9
		11	21	–38.27	92.39	112.5			27	53	38.27	–92.39	292.5
			22	–47.14	88.19	118.1				54	47.14	–88.19	298.1
		12	23	–55.56	83.15	123.8			28	55	55.56	–83.15	303.8
			24	–63.44	77.30	129.4				56	63.44	–77.30	309.4
2	4	13	25	–70.71	70.71	135.0	4	8	29	57	70.71	–70.71	315.0
			26	–77.30	63.44	140.6				58	77.30	–63.44	320.6
		14	27	–83.15	55.56	146.3			30	59	83.15	–55.56	326.3
			28	–88.19	47.14	151.9				60	88.19	–47.14	331.9
		15	29	–92.39	38.27	157.5			31	61	92.39	–38.27	337.5
			30	–95.69	29.03	163.1				62	95.69	–29.03	343.1
		16	31	–98.08	19.51	168.8			32	63	98.08	–19.51	348.8
			32	–99.52	9.80	174.4				64	99.52	–9.80	354.4

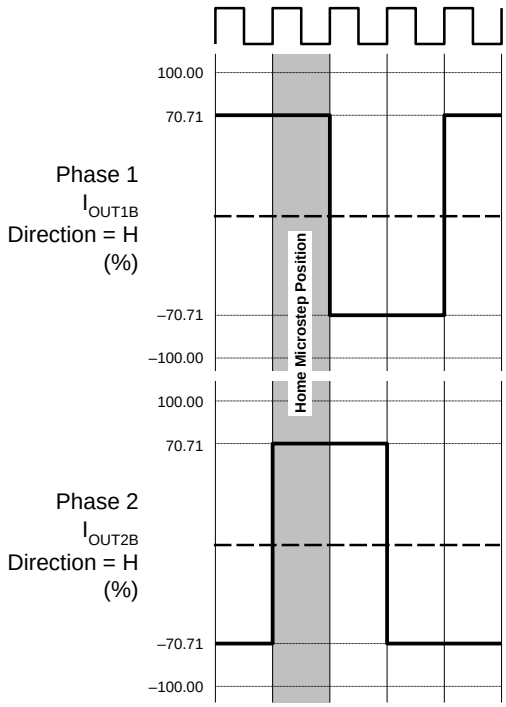


Figure 5. Full Step

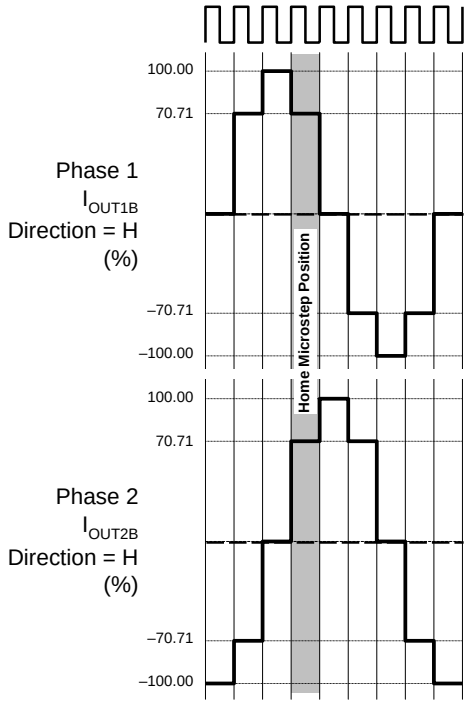


Figure 6. Half Step

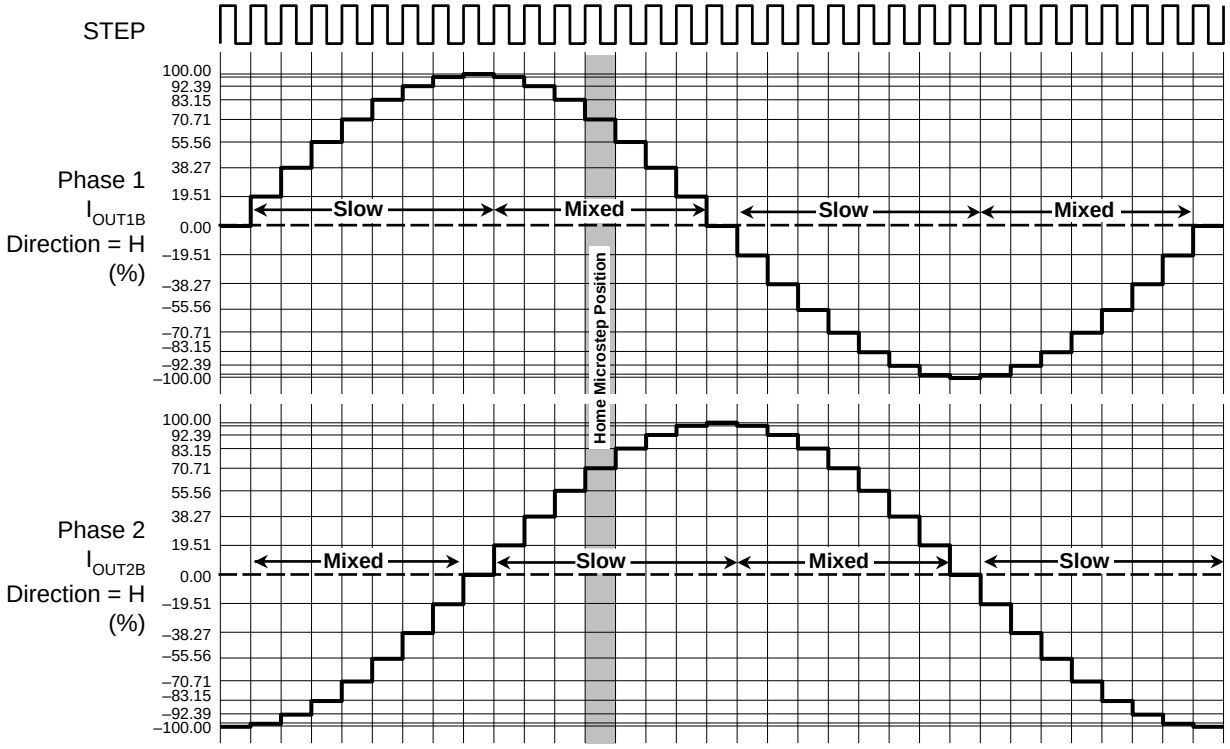


Figure 7. Eighth Step

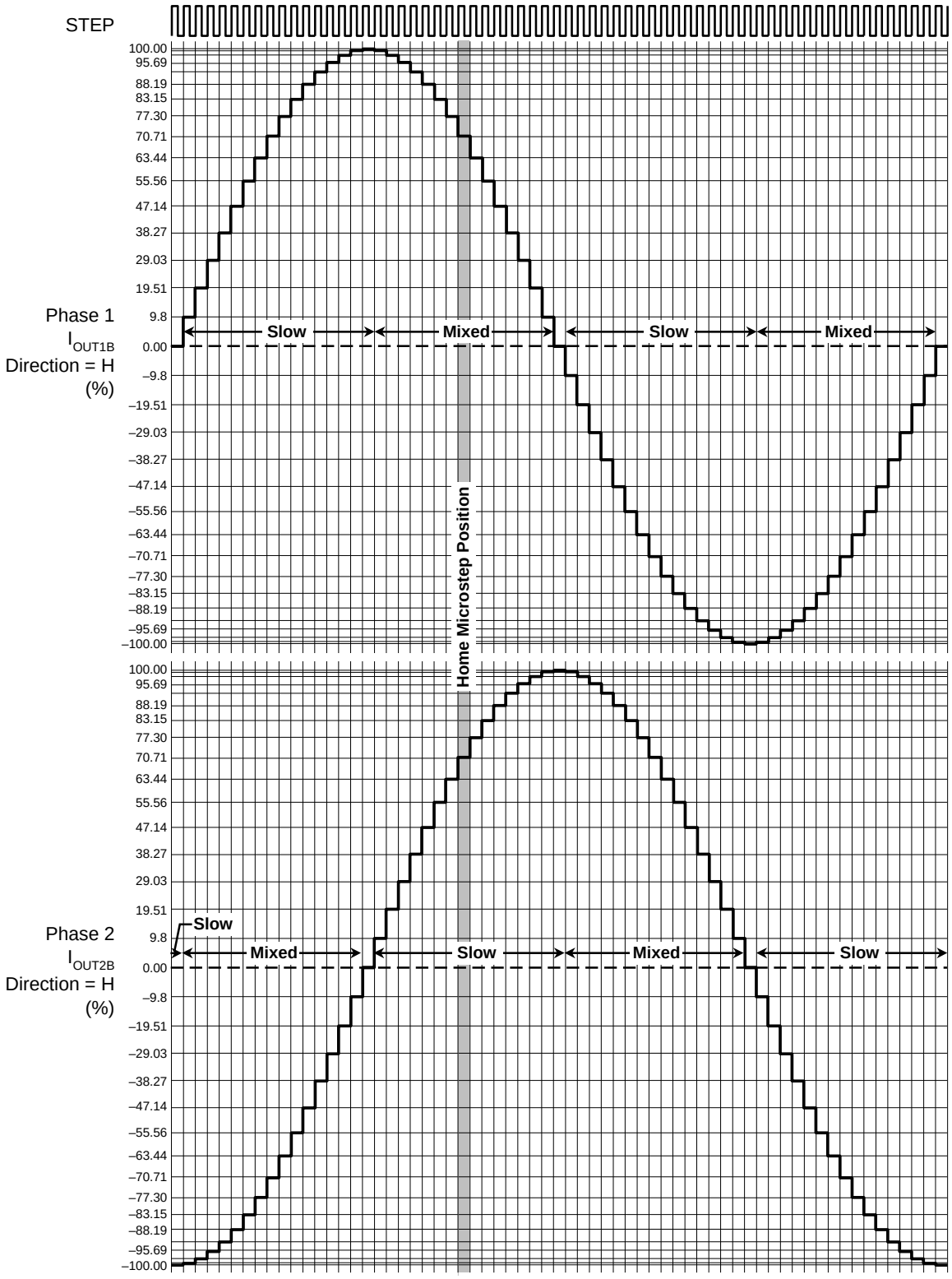


Figure 8. Sixteenth Steps

Functional Description

Device Operation. The A3980 is a complete microstepping motor driver with a built-in translator for easy operation with minimal control lines. It is designed to operate bipolar stepper motors in full-, half-, eighth-, and sixteenth-step modes. The currents in each of the two output full-bridges and all of the N-channel DMOS FETs are regulated with fixed off-time PMW (pulse width modulated) control circuitry. At each step, the current for each full-bridge is set by the value of its external current-sense resistor (R_{S1} or R_{S2}), a reference voltage (V_{REF}), and the output voltage of its DAC (which in turn is controlled by the output of the translator).

At power-up, the translator resets to the Home state, in which the motor is driven to the Home microstep position, where both phase currents are set to +70%. Then the translator sets the voltage regulator to mixed decay mode for both phases. When a step command signal occurs on the STEP input, the translator automatically sequences the DACs to the next level and current polarity. (See table 3 for the current-level sequence.) The microstep resolution is set by the combined effect of inputs MS1 and MS2, as shown in table 1.

When stepping, if the new output levels of the DACs are lower than their previous output levels, then the decay mode (fast, slow, or mixed decay) for the active full-bridge is set by the PFD input. If the new output levels of the DACs are higher than or equal to their previous levels, then the decay mode for the active full-bridge is set to slow decay. This automatic current decay selection improves microstepping performance by reducing the distortion of the current waveform that results from the back EMF of the motor.

Home Microstep Position. At power-up, or after a UVLO (undervoltage lockout) condition caused by low voltage on V_{DD}, the translator in the A3980 resets the motor to the Home microstep position. This corresponds to the 45° position, which is the step where both phase currents are +70%. Referring to table 3, for full-step mode this is step 1, for half-step this is step 2, for eighth-step this is step 5, and for sixteenth-step this is step 9. In table 3 and figures 5 through 8, the Home microstep position is indicated.

Step Input (STEP). A low-to-high transition on the STEP input sequences the translator and advances the motor one increment. The translator controls the input to the DACs and the direction of current flow in each winding. The size of the increment is determined by the combined state of inputs MS1 and MS2.

Microstep Select (MS1 and MS2). Selects the microstepping format, as shown in table 1. Any changes made to these inputs do not take effect until the next STEP rising edge.

Direction Input (DIR). This determines the direction of rotation of the motor. When low, the direction will be clockwise and when high, counterclockwise. Changes to this input do not take effect until the next STEP rising edge.

Internal PWM Current Control. Each full-bridge is controlled by a fixed off-time PWM current control circuit that limits the load current to a desired value, I_{TRIP}. Initially, a diagonal pair of source and sink DMOS FETs are enabled and current flows through the motor winding and the current sense resistor, R_S. When the voltage across R_S equals the DAC output voltage, the current sense comparator resets the PWM latch. The latch then turns off either the source DMOS (when in slow decay mode) or the sink and source DMOSs (when in fast or mixed decay modes).

The transconductance function is approximated by the maximum value of current limiting, $I_{TripMAX}$ (A), which is set by

$$I_{TripMAX} = V_{REF} / (8 \times R_S)$$

where R_S is the resistance of the sense resistor (Ω) and V_{REF} is the input voltage on the REF pin (V).

The DAC output reduces the V_{REF} output to the current sense comparator in precise steps, such that

$$I_{trip} = (\%I_{TripMAX} / 100) \times I_{TripMAX}$$

(See table 3 for $\%I_{TripMAX}$ at each step.)

It is critical that the maximum rating (0.5 V) on the SENSE pin is not exceeded. For full-step mode, V_{REF} can be applied up to the maximum rating of V_{DD}, because the peak sense value is 70% of maximum:

$$V_{REF} \times (0.707 / 8)$$

as shown in table 3. In all other modes, V_{REF} should not be allowed to exceed 4 V, because the peak sense value can reach V_{REF} / 8, or 100%.

Fixed Off-Time. The internal PWM current control circuitry uses a one-shot circuit to control the duration of time that the DMOS FETs remain off. The one shot off-time, t_{OFF}, is determined for each of the two phases by the combination of an external resistor (R_T) and a capacitor (C_T). One combination is connected from the timing terminal RC1 to ground, and the other similarly connected to RC2 . t_{OFF} (ns) is approximated by

$$t_{OFF} = R_T \times C_T$$

over a range of values from C_T= 470 pF to 1500 pF and from R_T = 12 kΩ to 100 kΩ.

RC Blanking. In addition to the fixed off-time of the PWM control circuit, the C_T component sets the comparator blanking time. This function blanks the output of the current sense comparators when the outputs are switched by the internal current control circuitry. The comparator outputs are blanked to prevent false overcurrent detection due to reverse recovery currents of the clamp diodes, and switching transients related to the capacitance of the load. The blank time, t_{BLANK} (ns), can be approximated by

$$t_{BLANK} = 1400 \times C_T$$

where C_T is the value of the capacitor C_T (nF).

The blank time should be as short as possible, without causing a false fault detection, to ensure that power dissipation during a fault condition is minimized. The blank time also defines the minimum duration of time that the full-bridge DMOS outputs cause the load current to rise. To ensure correct detection of motor faults, the minimum on-time is extended by an additional fault sampling time, t_{SCT}. The minimum on-time, t_{MINON} is then

$$t_{MINON} = t_{BLANK} + t_{SCT}$$

Charge Pump (CP1 and CP2). The charge pump is used to generate a gate supply greater than that of VBB for driving the source-side DMOS gates. A 100 nF ceramic capacitor (C_{CP}), capable of withstanding the battery voltage VBATT, should be connected between CP1 and CP2. In addition, a 100 nF ceramic capacitor (C_{CS})is required between VCP and VBB, to act as a reservoir for operating the high-side DMOS devices. The voltage on C_{CS} is limited to the charge pump voltage, which is always less than 10 V.

VREG (VREG). This internally-generated voltage is used to operate the sink-side DMOS FETs. The VREG terminal must be decoupled with a 220 nF (10V) capacitor to ground. VREG is internally monitored. In the case of a fault condition, the DMOS outputs of the A3980 are disabled.

Enable Input (ENABLE). This input simply turns off all of the DMOS outputs. When set to a logic high, the outputs are disabled. When set to a logic low, the internal control enables the outputs as required. The translator inputs (STEP, DIR, MS1, and MS2), as well as the internal sequencing logic, all remain active, independent of the ENABLE input state.

Sleep Mode (SLEEP). To minimize power consumption when the motor is not in use, this input disables much of the internal circuitry including the output DMOS FETs, voltage regulator, and charge pump. A logic low on the SLEEP terminal puts the A3980 into Sleep mode. A logic high allows normal operation, as well as start-up (at which time the A3980 drives the motor to the Home microstep position).

Percent Fast Decay Input (PFD). When a STEP input signal commands an output current level that is lower than that of the previous step, it switches the output current decay to slow, fast, or mixed decay mode, depending on the voltage level at the PFD input, as shown in the following table.

Lower PFD Input Voltage Level	Decay Mode
$V_{PFD} > (0.6 \times V_{DD})$	Slow
$(0.21 \times V_{DD}) \le V_{PFD} \le (0.6 \times V_{DD})$	Mixed
$V_{PFD} < (0.21 \times V_{DD})$	Fast

Mixed Decay Operation. Depending on the step sequence, if the voltage on the PFD pin is between $0.6 \times V_{DD}$ and $0.21 \times V_{DD}$, the full-bridge can operate in

mixed decay mode, as shown in figures 5 through 8. As the trip point is reached, the A3980 goes into fast decay mode until the voltage on the RC pin decays to the same level as the voltage applied to the PFD pin. The duration of time that the bridge operates in fast decay mode, t_{FD} (ns), is estimated by

$$t_{FD} = R_T \times C_T \times \ln[0.6\,(V_{DD} / V_{PFD})]$$

over a range of values from C_T= 470 pF to 1500 pF and from R_T = 12 kΩ to 100 kΩ.

After this fast decay period, the A3980 switches to slow decay mode for the remainder of the fixed off-time period.

Synchronous Rectification. When a PWM-off cycle is triggered by an internal fixed-off-time cycle, load current recirculates according to the decay mode selected by the control logic. The synchronous rectification feature turns on the appropriate FETs during current decay, and effectively shorts out the body diodes with the low DMOS R_{DSON}. This reduces power dissipation significantly, and eliminates the need for external Schottky diodes. Synchronous rectification has two modes: Active mode and Disabled mode (described below).

Active Mode. When the input on the SR terminal is set at logic low, Active mode is enabled. This mode allows synchronous rectification to occur, but when a zero current level is detected, it also prevents reversal of the load current by turning off synchronous rectification. This prevents the motor winding from conducting in the reverse direction.

Disabled Mode. When the input on the SR terminal is set at logic high, Disabled mode takes effect. This mode disables synchronous rectification. This mode is typically used when external diodes are required to transfer power dissipation from the A3980 package to the external diodes.

Shutdown. In the event of an overtemperature fault or an undervoltage fault on VREG, the DMOS outputs of the A3980 are disabled until the fault condition is removed. In the case of an overvoltage fault, the sink DMOS FETs are switched on, and the source FETs off. At power-up, and in the event of low V_{DD}, the UVLO circuit disables the DMOS outputs until V_{DD} reaches the minimum level. Once V_{DD} is above the minimum level, the translator resets to the Home state and the DMOS outputs are re-enabled.

Thermal Protection. All drivers are turned off when the junction temperature reaches the thermal shutdown value, typically 170°C. This is intended only to protect the A3980 from failures due to excessive junction temperatures. Thermal protection will not protect the A3980 from continuous short circuits, and additional fault diagnostics are integrated for this purpose. Thermal shutdown has a hysteresis of approximately 15°C.

Diagnostic Features. The A3980 includes monitor circuits that can detect shorts to VBB, shorts to ground, and shorted or open circuit load. Short circuits are detected by monitoring the voltage across the driving DMOS FETs and the open load is detected by monitoring the phase current when the motor is in the Home microstep position. All fault detection takes place following a delay after the blank time.

Short to VBB. A short from any of the motor connections to the battery or VBB connection is detected by monitoring the voltage across the bottom FETs in each full-bridge. When the FET is on, the voltage should be no greater than the V_{DSLT} value defined in the Electrical Characteristics table.

Short to Ground. A short from any of the motor connections to ground is detected by monitoring the voltage across the top FETs in each full-bridge. When the FET is turned on, the voltage should be no greater than the V_{DSHT} value defined in the Electrical Characteristics table.

Shorted Load. A short across the load is detected by monitoring the voltage across both the top and bottom FETs in each full-bridge.

Short Fault Operation. Because motor capacitance may cause the measured voltages to show a fault as the full-bridge switches, voltages are not sampled until after the blank time plus an internally-generated delay, t_{SCT}. Once a short circuit has been detected, all outputs for the faulty phase are disabled until the next step command. At the next step command, the outputs are re-enabled and the voltage across the FET is resampled.

While the fault persists, the A3980 continues this cycle at each step command: enabling the outputs for a short period, and then disabling the outputs. This allows the A3980 to handle a continuous short circuit without damage. If, while stepping rapidly, a short circuit appears and no action is taken, the repeated short-circuit current pulses eventually cause the temperature of the A3980 to rise and an overtemperature fault occurs.

Low Load Current Fault Operation. A low load current is detected by monitoring the measured phase current in each output while driving the motor in the Home microstep position. At the Home microstep position, each phase current should reach 70% of $I_{TripMax}$. If either phase current does not exceed half of this expected value (more than 35% of $I_{TripMax}$) while in the Home microstep position, then a low load current condition is reported on the next rising edge of the STEP input. If the measured current in both phases exceeds 35% of $I_{TripMax}$) then no fault will be generated on the next rising edge of the STEP input.

If an open load condition appears while stepping, then it is detected after the translator cycles through the Home state. Although the A3980 continues to drive the DMOS outputs during an open load condition, it does not clear the fault flags until the next Home state occurs.

There are two conditions that can cause a low load current. The first is an open circuit on either or both motor phase connections. In this condition, current can never flow through the phase so a low load current will always be flagged. The second condition is where the back EMF of the motor limits the phase current to less than the low load current trip level. This will happen when the stepper motor is running close to its limiting speed. To confirm an open load condition when a low load current is flagged, the step rate should be reduced to a level below half the maximum step rate. If the low load current flag remains active at the lower step rate, after completing the number of steps required to pass the home condition, then an open circuit condition is confirmed.

To allow immediate detection of an open load condition at power up or after coming out of sleep mode, the A3980 translator is reset to the Home microstep position and the low load current fault flags are set. If no open load condition exists then the fault flags will be reset on the next rising edge of the STEP input.

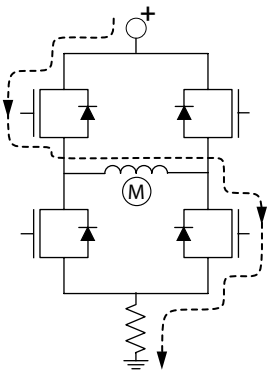
Supply Monitors. External and internal supplies are monitored to ensure that they are within the correct operating range. If the main supply exceeds the overvoltage limit, V_{OVB}, the fault flags are set and the A3980 enters a safety mode in which all low-side DMOS FETs are enabled and all high-side DMOS FETs are disabled. This allows the A3980 to survive a load dump transient condition that has up to 50 V on VBATT and a duration of up to 500 ms. If the internal regulator V_{REG} or the logic supply V_{DD} go below their respective undervoltage limits (V_{UVR} or V_{UVD}), then: the fault flags are set, the DMOS outputs are disabled, and the internal logic is reset to the power-on state (the translator is set to the Home state).

Diagnostic Fault Flags (FF1, FF2). Diagnostic fault conditions are reported using the two fault flag outputs (open drain). These are active-low outputs which are coded as shown in table 2 to discriminate between the fault conditions. When both fault flags are high, no fault exists.

Application Information

The A3980 is a power circuit, therefore careful consideration must be given to power dissipation and the effects of high currents on interconnect and supply wiring.

Power Dissipation. A first order approximation of the power dissipation in the A3980 can be determined by examining the power dissipation in each of the two full-bridges during each of the operation modes. When synchronous rectification is used, current flow most of the time through the DMOS FETs that are switched on. When synchronous rectification is not used, the current flows through the body diode of the DMOS FETs during the decay phase. The use of fast or slow decay also affects the dissipation. All the above combinations can be calculated from five basic DMOS output states, shown in the following illustrations.



Drive Current Ramp

Diagonally opposite DMOS output transistors are on. Current flows from positive supply through load to ground. Used in all combinations.

Dissipation is I^2R losses in the DMOS transistors:

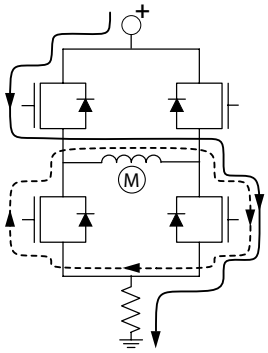
$$P_D = I^2 (R_{DSONH} + R_{DSONL})$$

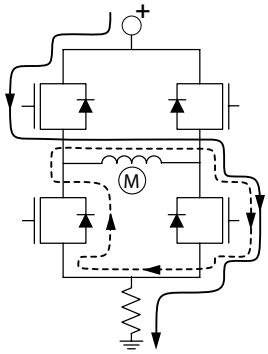
Synchronous Slow Decay

Both low-side DMOS output transistors are on. Current circulates through both transistors and the load.

Dissipation is I^2R losses in the DMOS transistors:

$$P_{SS} = I^2 (2 \times R_{DSONL})$$





Non-Synchronous Slow Decay

One low-side DMOS output transistor and one body diode conducting. Current circulates through the diode, the transistor, and the load.

Dissipation is I^2R losses in the DMOS transistors plus IV loss in the diode:

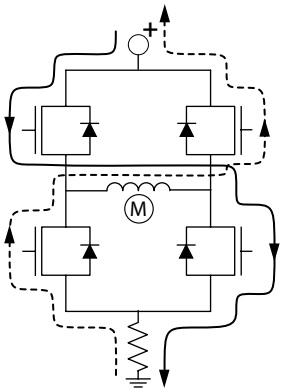
$$P_{NS} = (I^2 \times R_{DSONL}) + (I \times V_F)$$

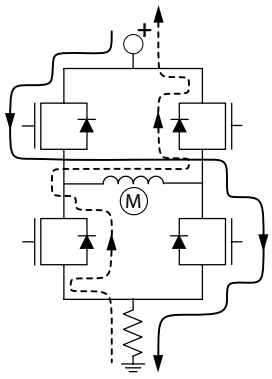
Synchronous Fast Decay

Diagonally opposite DMOS output transistors are on. Current flows from ground through load to positive supply.

Dissipation is I^2R losses in the DMOS transistors:

$$P_{SF} = I^2 (R_{DSONH} + R_{DSONL})$$





Non-Synchronous Fast Decay

Diagonally opposite body diodes conducting. Current flows from ground through load to positive supply.

Dissipation is IV losses in the diodes:

$$P_{NF} = I (V_{FH} + V_{Fl})$$

The total dissipation for each of the four decay modes is the average power for the current ramp and the current decay portions of the PWM cycle.

For slow decay, the current is rising for approximately 20% of the cycle and decaying for approximately 80%. For fast decay, the ratio is approximately 50% for each. Note that these are approximate figures, and they vary slightly depending on the motor characteristics and the use of synchronous rectification.

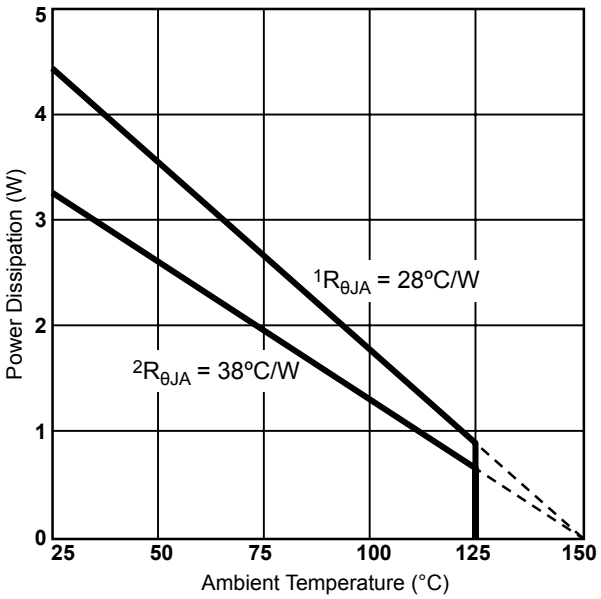
The power dissipation, P_{TOT}, in each decay mode can be calculated as shown in the following formulas.

Synchronous slow decay mode:

$$P_{TOT} = (0.2 \times P_D) + (0.8 \times P_{SS})$$

$$P_{TOT} = [0.2 \times I^2 (R_{DSONH} + R_{DSONL})] + [0.8 \times I^2 (2 \times R_{DSONL})]$$

Allowable Package Power Dissipation



[1]$R_{\theta JA}$ at 28°C/W measured on a JEDEC-standard "High-K" 4-layer PCB.

[2]$R_{\theta JA}$ at 38°C/W measured on a typical 2-sided PCB with 3 in.^{2} (1935 mm^2) copper ground area.

Non-synchronous slow decay mode:

$$P_{TOT} = (0.2 \times P_D) + (0.8 \times P_{NS})$$

$$P_{TOT} = [0.2 \times I^2 (R_{DSONH} + R_{DSONL})] + \{0.8 \times [I^2 R_{DSONL} + (I \times V_F)]\}$$

Synchronous fast decay mode:

$$P_{TOT} = (0.5 \times P_D) + (0.5 \times P_{SF})$$

$$P_{TOT} = I^2 (R_{DSONH} + R_{DSONL})$$

Non-synchronous fast decay mode:

$$P_{TOT} = (0.5 \times P_D) + (0.5 \times P_{NF})$$

$$P_{TOT} = [0.5 \times I^2 (R_{DSONH} + R_{DSONL})] + (0.5 \times I^2 \times R_{DSONL})$$

An approximation of the total dissipation can be calculated by summing the total power dissipated in both full-bridges and adding the control circuit power due to $V_{BB} \times I_{BB}$ and $V_{DD} \times I_{DD}$. The total power at the required ambient temperature can then be compared to the allowable power dissipation, shown in the Allowable Package Power Dissipation chart.

For critical applications, where the first order power estimate is close to the allowable dissipation, the power calculation should take several other parameters into account including: motor parameters, dead time, and switching losses in the controller.

Layout. The printed circuit board should use a heavy ground plane. For optimum electrical and thermal performance, the A3980 should be soldered directly onto the board. The load supply terminal, V_{BB}, should be decoupled with an electrolytic capacitor (>47 µF is recommended), placed as close to the A3980 as possible. To avoid problems due to capacitive coupling of the high dv/dt switching transients, route the full-bridge output traces away from the sensitive logic input traces. Always drive the logic inputs with a low source impedance to increase noise immunity.

Grounding. A star ground system located close to the A3980 is recommended. On the 28-lead TSSOP package, the analog ground (lead 7) and the power ground (lead 21) must be connected together externally. The copper ground plane located under the exposed thermal pad is typically used as the star ground point.

Current Sensing. To minimize inaccuracies caused by ground-trace IR drops in sensing the output current level, the current-sense resistors (R_{S1} and R_{S2}) should have an independent ground return to the star ground point. This path should be as short as possible. For low-value sense resistors, the IR drops in the printed circuit board sense resistor traces can be significant and should be taken into account. The use of sockets should be avoided as they can introduce variation in R_S due to their contact resistance.

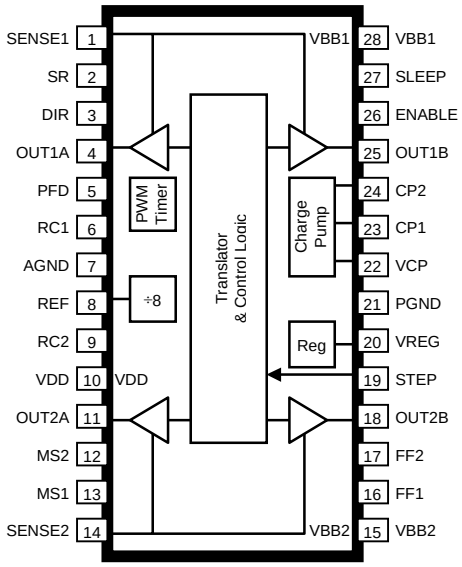
The recommended value of the sense resistor, R_S (Ω), is given by

$$R_S = 0.5 / I_{TripMAX}$$

up to a maximum of 1 Ω for $I_{TripMAX}$ of 0.5 A. Below 0.5 A, R_S should be 1 Ω, and V_{REF} reduced accordingly, as shown in the following table.

I_{MAX} (A)	Recommended	
	R_S(Ω)	V_{REF}(V)
0.1	1.00	0.8
0.2	1.00	1.6
0.3	1.00	2.4
0.4	1.00	3.2
0.5	1.00	4.0
0.6	0.83	4.0
0.7	0.71	4.0
0.8	0.63	4.0
0.9	0.56	4.0
1.0	0.50	4.0

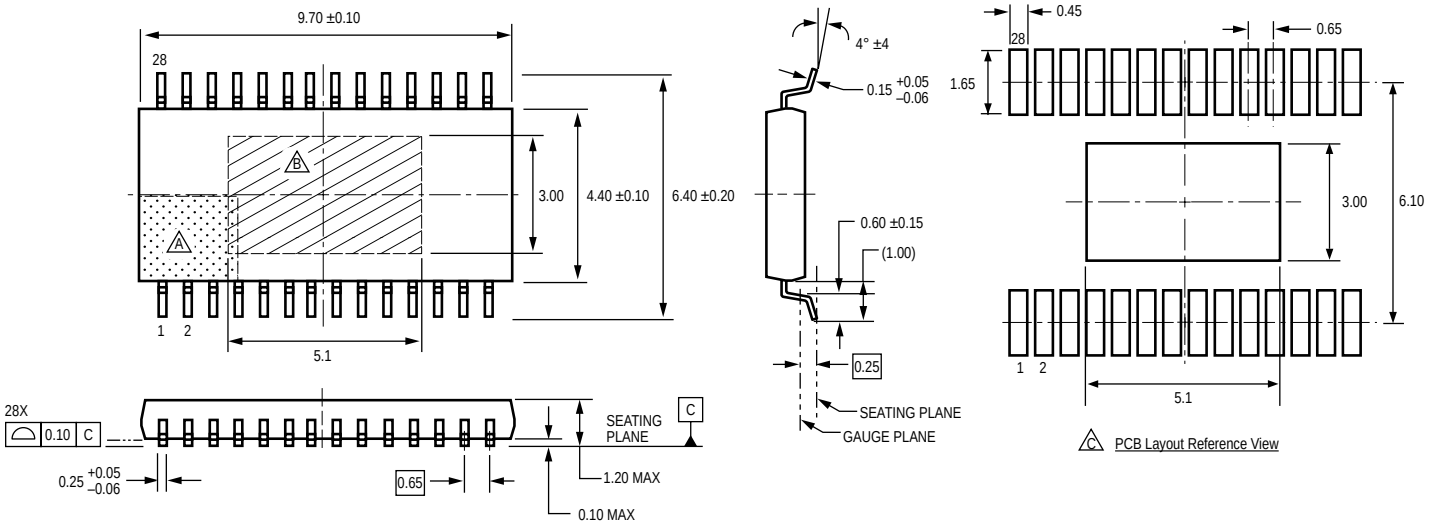
Pin-out Diagram



Terminal List Table

Name	Description	Number
SENSE1	Sense resistor for full-bridge 1	1
SR	Enable synchronous rectification	2
DIR	Logic input	3
OUT1A	Output A for for full-bridge 1	4
PFD	Mixed decay setting	5
RC1	Analog input for fixed off-time for full-bridge 1	6
AGND	Analog ground	7
REF	Current trip reference voltage input	8
RC2	Analog input for fixed off-time for full-bridge 2	9
VDD	Logic supply voltage	10
OUT2A	Output A for for full-bridge 2	11
MS2	Logic input	12
MS1	Logic input	13
SENSE2	Sense resistor for full-bridge 2	14
VBB2	Load supply 2	15
FF1	Fault flag 1	16
FF2	Fault flag 2	17
OUT2B	Output B for for full-bridge 2	18
STEP	Logic input	19
VREG	Regulator decoupling	20
PGND	Power ground	21
VCP	Reservoir capacitor	22
CP1	Charge pump capacitor 1	23
CP2	Charge pump capacitor 2	24
OUT1B	Output B for for full-bridge 1	25
ENABLE	Logic input	26
SLEEP	Logic input	27
VBB1	Load supply 1	28

Pacakge LP, 28-Pin TSSOP with Exposed Thermal Pad



For reference only
(reference JEDEC MO-153 AET)
Dimensions in millimeters
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions
Exact case and lead configuration at supplier discretion within limits shown

A Terminal #1 mark area

B Exposed thermal pad (bottom surface)

C Reference land pattern layout (reference IPC7351 SOP65P640X120-29CM); All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances; when mounting on a multilayer PCB, thermal vias at the exposed thermal pad land can improve thermal dissipation (reference EIA/JEDEC Standard JESD51-5)

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